#4

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Schiavone, et al.

Serial No.: 09/462,716

Filed: January 10, 2000

For: **METHOD FOR MINIMIZING THE CORNER EFFECT BY DENSIFYING THE INSULATING LAYER**

§ Examiner: Unknown
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§ Group Art Unit: Unknown
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§ Atty. Docket No. 5310-02200/EBM
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CERTIFICATE OF MAILING
37 C.F.R. § 1 8

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Date — Katherin L. Cope

ELECTION UNDER 37 C.F.R. §§ 3.71 and 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, being Assignee of record of the entire interest in the above-identified application by virtue of an assignment recorded in the United States Patent and Trademark Office as set forth below, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventors.

The Assignee hereby revokes any previous Powers of Attorney and appoints:

Dan R. Christen	Reg. No. 39,943
Gentry E. Crook	Reg. No. 44,633
Kevin L. Daffer	Reg. No. 34,146
Mark R. DeLuca	Reg. No. 44,649
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Louise K. Miller	Reg. No. 36,609
David W. Quimby	Reg. No. 39,338
Doug Shamah	Reg. No. 45,093
Larry D. Thompson	Reg. No. 43,952

each an attorney or agent of the firm of CONLEY, ROSE & TAYON, P.C., as its attorney or agent for so long as they remain with such firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned has reviewed the evidentiary documents, specifically the Assignment to France Telecom, referenced below, and certify that to the best of my knowledge and belief, title remains in the name of the Assignee.

Please direct all communications as follows:

Eric B. Meyertons, Esq.
CONLEY, ROSE & TAYON, P.C.
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AUSTIN, TEXAS 78767-0398
(512) 476-1400 (voice)
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ASSIGNEE:

FRANCE TELECOM

FRANCE TÉLÉCOM 6, place d'Alleray 75015 PARIS

By: _____

Name: D. LEMOYNE

Title: Corporate Patents Manager

Date: September 6, 2000

ASSIGNMENT: x Enclosed for recording

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty. Dkt. No: 5310-02200

Inventor(s): Patrick Schiavone
Frédéric Gaillard

Title: METHOD FOR MINIMIZING THE CORNER EFFECT BY Ddensifying THE INSULATING LAYER

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UNDER 37 C.F.R. §1.10

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DATE OF DEPOSIT: January 10, 2000

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Debra J. Tix

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

INTERNATIONAL APPLICATION NO.: PCT/FR98/01475
INTERNATIONAL FILING DATE: July 8, 1998
PRIORITY DATE CLAIMED: July 8, 1997
U.S. APPLICATION NO. (If known):

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. § 371.

2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. § 371.

3. ☐ This is an express request to begin national examination procedures (35 U.S.C. § 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. § 371(b) and PCT Articles 22 and 39(l).

4. ☒ A translation of the International Application into English (35 U.S.C. § 371(c)(2)), including: a title page; 6 page(s) of specification; 1 page(s) of claims (claims 1-4); 1 page(s) of abstract.

5. ☒ Drawings
☒ Formal Figure(s) 1-2 on 1 sheet(s).

6. ☒ A copy of the International Application as filed (35 U.S.C. § 371(c)(2))
☒ is transmitted herewith (15 pages).
☐ has been transmitted by the International Bureau.
☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. § 371(c)(3))
   - ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   - ☐ have been transmitted by the International Bureau.
   - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. § 371(c)(3)).

9. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
   - ☐ A copy of the Demand for International Preliminary Examination is enclosed.

10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. § 371(c)(4)):
   - ☐ is enclosed (_____ pages).
   - ☐ a combined Declaration and Power of Attorney is enclosed (2 pages).
   - ☒ is not enclosed. Applicant requests the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail. Further, Applicant requests that the NOTICE OF MISSING PARTS-FILING DATE GRANTED be sent to the undersigned representative of Applicant.

11. ☒ Applicant hereby claims priority to:
   - ☒ International Application No.: PCT/FR98/01475 filed July 8, 1998.
   - ☒ French application No.: 97/08642 filed July 8, 1997.

12. ☐ A translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. § 371(c)(5)).

13. ☒ The entire disclosure of the International Application referred to above is considered to be part of the accompanying application and is hereby incorporated by reference herein.

14. ☐ Assignment Papers.
   - ☐ An assignment document is enclosed for recording (2 pages).
   - ☐ Form PTO-1595 Assignment Recordation Cover Sheet (1 page).

15. ☒ A Preliminary Amendment (2 pages).

16. ☐ A substitute specification for pages _____ (_____ pages).

17. ☐ Power of Attorney
   - ☐ Is enclosed.
   - ☐ a combined Declaration and Power of Attorney is enclosed.

18. ☐ Information Disclosure Statement (IDS), including:
   - ☐ Form PTO-1449
   - ☐ Reference(s) marked according to Form PTO-1449.

19. ☒ Return Receipt Postcard

20. ☐ Small Entity Status
   - ☐ A small entity statement is enclosed.

21. ☒ Copy of PCT Form PCT/IB/301.

22. ☒ Copy of PCT Form PCT/IB/304.

23. ☒ Copy of PCT Form PCT/IB/308.

24. ☒ Copy of PCT Form PCT/IB/332

25. ☐ Copy of PCT Form PCT/IB/338

26 ☐ Copy of International Request.

27. ☒ Copy of International Preliminary Examination Report.
☒ A copy of the International Preliminary Examination Report in French.
☐ English Translation of the International Preliminary Examination Report.

28. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR § 1.492 (a) (1)-(5):				
☐ Neither international preliminary examination fee nor international search fee paid to USPTO and International Search Report not prepared by the EPO or JPO.....$970.00				
☒ International preliminary examination fee not paid to USPTO but International Search Report prepared by the EPO or JPO.....$840.00				
☐ International preliminary examination fee not paid to USPTO but international search fee paid to USPTO.....$760.00				
☐ International preliminary examination fee paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4).....$670.00				
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Surcharge of $130.00 for furnishing oath or declaration later than ☐ 20 ☐ 30 Months from the earliest claimed priority date (37 C.F.R. § 1.492(e)).				
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	4 - 20 =	0	x $18.00 =	
Independent claims	1 - 3 =	0	x $78.00 =	
MULTIPLE DEPENDENT CLAIM(S)			+ $260.00 =	
TOTAL OF ABOVE CALCULATIONS:				$840.00
Reduction by 50% for Small Entity. A Small Entity Statement must be filed:				
SUBTOTAL:				$840.00
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 Months from the earliest claimed priority date:				
TOTAL NATIONAL FEE:				
Fee for recording the enclosed assignment. The assignment must be accompanied by an appropriate cover sheet. $40.00 per property:				
TOTAL FEES ENCLOSED:				

☒ A check in the amount of $840.00 is enclosed.

☐ Please charge my Deposit Account No. 03-2769/ in the amount of to cover the above fees.

☒ The Commissioner is hereby authorized to charge any other fees which may be required or credit any overpayment to Conley, Rose, & Tayon, P.C., Deposit Account No. 03-2769/5310-02200/EBM.

Address all future correspondence to:
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Signature

Name Mark R. DeLuca
Registration No. 44,649
Date January 10, 1999

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: Unknown
Filed: Herewith
Inventor(s):
Patrick Schiavone
Frédéric Gaillard

Title: METHOD FOR MINIMIZING THE CORNER EFFECT BY Ddensifying THE INSULATING LAYER

Examiner: Unknown
Group/Art Unit: Unknown
Atty. Dkt. No: 5310-02200

CERTIFICATE OF EXPRESS MAIL
UNDER 37 C.F.R. §1.10

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DATE OF DEPOSIT. January 10, 1999

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Box Patent Application
Washington, DC 20231

Debbie Tix

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-captioned application as follows:

In the Claims:

Please amend the claims as follows:

4. (amended) Method according to [any of claims 1 to 3] claim 1, [characterized in that] wherein the layer [(23)] of silicon oxide deposited in the trenches [(26)] is densified directly after depositing said layer, before flattening it.

It is believed that no fees are due in connection with the filing of this Preliminary Amendment. However, if any fees are due, the Assistant Commissioner is hereby authorized to deduct said fees from Conley, Rose & Tayon Deposit Account No. 03-2769/5040-02301/EBM.

Respectfully submitted,

Mark R. DeLuca
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Debra J. Tix

METHOD FOR MINIMIZING THE CORNER EFFECT BY Ddensifying THE INSULATING LAYER

By:

Patrick Schiavone

Frédéric Gaillard

5310-02200

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The invention concerns integrated circuit fabrication technologies and in particular the production of MOS transistors.

In existing small dimensional technologies, shallow trench insulation (STI) (or BOX) techniques are preferably used for lateral insulation of active areas and in particular lateral insulation of MOS transistors. These techniques combine etching trenches disposed laterally relative to the future active areas and filling said trenches with an insulative material such as silicon oxide. The insulative layer is flattened before depositing the gate when manufacturing MOS transistors. The trenches are generally filled by depositing the insulative material onto a previously formed layer of thermal oxide.

The successive oxidation and sacrificial deoxidation operations of the insulation method which precede the deposition of the gate tend to uncover so-called "corner" areas of the future active areas. The expression "corner area" therefore refers to the abrupt transition between an insulation area and an active area. Uncovering them is significantly accentuated if some of the insulative oxide is consumed during the operation of flattening the insulative layer filling the trenches.

The appearance of these "corner" areas encourages concentration of the field lines at the top corner of the active area and thus the formation of a spurious transistor. Three transistors are therefore formed, namely the main transistor in the centre and two spurious "corner" transistors. The latter have a lower threshold voltage than the main transistor and therefore begin to conduct before it. This phenomenon leads to an increase in the current consumed before effective operation of the

transistor.

One way to improve the electrical qualities of the lateral insulation and in particular the concentration of the field lines in the corner areas at the top corners of the active area is to maintain the oxide at the same level as the active area. The oxide deposited must therefore have a density close to that of the silica. Given the structure of silicon oxides (xerogel structure) used for filling shallow trenches, it is necessary to anneal them at a very high temperature (> 1 200°C) or to use some other technique with a very low thermal balance to densify them.

It is therefore necessary to determine a way to eliminate or at least significantly reduce this unwanted "corner" effect.

The inventors have now discovered that it is possible to reduce significantly the "corner" effect that has previously degraded the electrical properties of MOS transistors without inducing additional problems into the manufacture of such transistors.

The object of the invention is therefore a method of minimizing the "corner" effect in shallow trenches of silicon oxide for lateral insulation of active areas, whose essential feature is the densification of the layer of silicon oxide deposited in said lateral trenches.

These silicon oxides are densified in accordance with the invention by irradiating said insulative layer with short wavelength light. This technique maintains a low thermal balance of the operation.

The technique has the additional advantage that it can easily be used within an MOS transistor fabrication process.

According to a preferred aspect of the invention, the insulative oxide layer is irradiated with light at a wavelength less than or equal to 200 nm with a number of

photons per cm^2 greater than 10^{19} and an energy at least equal to 9 eV.

More particularly, the light used has a wavelength of approximately 100 nm.

The oxide layer deposited in the insulating trenches can be densified directly after depositing the insulative layer or after flattening it.

To prevent the "corner" area being uncovered during flattening of the insulative oxide deposited in the trenches, the densification is preferably performed directly after depositing the oxide into the shallow trenches.

Other advantages and features of the invention will become apparent on examining the following detailed description of embodiments of the invention, which is given by way of non-limiting example only, and the accompanying drawings, in which:

Figure 1 is a diagram showing an MOS transistor manifesting the "corner" effect, and

Figure 2 is a diagram showing a device in accordance with the invention before depositing the gate.

In figure 1, an active area 1 has received lateral insulation by a prior art method, after which a gate 5 has been deposited on said active area in order to form an MOS transistor.

The conventional process forms shallow trenches laterally relative to a predetermined area intended subsequently to form an active area 1 of the semiconductor device. A thin layer 2 of thermal oxide is then applied to the flanks and the bottom of the trench, which constitutes a good interface between the substrate of the active area and the insulation. The next step consists in depositing a layer 3 of silicon oxide into the trenches to fill them. The active areas are generally protected during this process by a protective

mask deposited onto the surface of said active areas. This is why, after flattening the oxide layer and removing the mask protecting the active areas, the height of the oxide layer 3 deposited in the lateral trenches is slightly greater than the height of the active area 1.

The steps of the process of fabricating the semi-conductor device uncover the top corners of the active area 1. A thin oxide gate layer 4 is formed on the semi-conductor device, onto which the gate 5 is deposited, overlapping the insulation area. The process of fabricating the MOS transistor then continues in the conventional manner. When the transistor obtained is activated, concentration of the field lines in the "corner" areas is observed and leads to the formation of two spurious transistors at respective ends of the gate.

Figure 2 shows the semi-conductor device obtained by the method of the invention in the step immediately preceding the formation of the gate oxide and the deposition of the gate. Note that no "corner" areas have been uncovered, in contrast to the previous figure.

After etching trenches 26 disposed laterally relative to the future active areas 21 (only one of which is shown in the figure), using a conventional process, a layer 22 of thermal oxide is formed on the walls and the bottom of the trenches and the surface of the active areas 21. At least one insulative silicon oxide layer 23 is then deposited in the trenches 26 in a conventional manner, for example by CVD. The thickness of this layer is such that all the trenches of the wafer are filled perfectly.

The future active areas are usually covered with a protective mask during the insulation process to keep their surface intact. The thickness of the insulation deposited in the trenches is then at least equal to the height of the active area (depth of the trenches) covered

with the thermal oxide and the protective mask.

In one embodiment of the invention, the next step is the essential feature of the invention. It consists in densifying the layer 23 of silicon oxide deposited in the trenches 26.

In another embodiment of the invention the insulative layer 23 of silicon oxide is conventionally flattened before densifying it, for example by mechanical/chemical polishing. The densification step is then performed on the flattened oxide layer.

At whichever stage the insulative layer 23 of silicon oxide is densified, in accordance with one particular feature of the invention the densification can be done by irradiating said layer with short wavelength light (e.g. a laser beam or light from a mercury lamp).

The light used for this irradiation generally has a wavelength less than or equal to 200 nm with a number of photons per cm^2 of 10^{19} and an energy at least equal to 9 eV. Optimum densification is obtained when the wavelength is around 100 nm. The silicon oxide layer 23 deposited in the trenches 26 is thus converted into a denser insulative layer having a structure similar to that of pure silica.

After the densification step, the insulation and MOS transistor fabrication process continues in the conventional manner. Figure 2 shows diagrammatically the state of the device obtained after flattening the oxide layer, removing the protective masks from the future active areas and deoxidizing the surfaces. A future active area 21 is therefore insulated laterally on each side by shallow trenches 26. The trenches are coated with a thermal oxide layer 22 and filled with at least one flattened insulative layer 23 of densified silicon oxide having a density close to that of the thermal oxide.

The transistor fabrication process then continues in the conventional manner.

The aggressive effect of the successive steps of flattening the insulative layer filling the trenches, removing the protective masks, deoxidizing the surface of the future active areas, etc. is thereby minimized. The "corner" areas of the future active areas are no longer uncovered, as they were previously. When a transistor whose shallow trench insulated areas have been densified in accordance with the invention is activated, there is no longer any concentration of field lines in the "corner" areas. The spurious effect referred to as the "corner" effect is minimized and the electrical properties of MOS transistors made this way are significantly improved without inducing other defects or drawbacks in the manufactured devices.

The method of the invention also has the advantage that it can easily be used on an MOS transistor fabrication line using conventional plant.

CLAIMS

1. Method of minimizing the "corner" effect in shallow trenches (26) of silicon oxide for laterally insulating active areas (21), characterized in that after depositing a layer (23) of silicon oxide into the trenches (26), said deposited layer is densified by irradiation with short wavelength light.

2. Method according to claim 1, characterized in that the oxide layer is densified by irradiating said layer with light at a wavelength less than or equal to 200 nm with a number of photons per cm^2 greater than 10^{19} and an energy at least equal to 9 eV.

3. Method according to claim 2, characterized in that the wavelength of the light is approximately 100 nm.

4. Method according to any of claims 1 to 3, characterized in that the layer (23) of silicon oxide deposited in the trenches (26) is densified directly after depositing said layer, before flattening it.

FIG.1

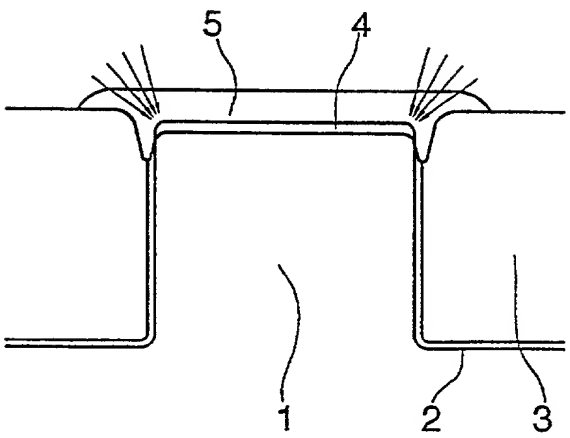

FIG.2